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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,530	03/10/2004	Ramachandra Divakaruni	FIS920030421US1	2529

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INTERNATIONAL BUSINESS MACHINES CORPORATION
DEPT. 18G
BLDG. 300-482
2070 ROUTE 52
HOPEWELL JUNCTION, NY 12533

EXAMINER	
DANG, PHUC T	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 07/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

SM

Office Action Summary	Application No.	Applicant(s)	
	10/708,530	DIVAKARUNI ET AL.	
	Examiner	Art Unit	
	PHUC T. DANG	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *election filed on June 21, 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G: 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *12-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4 and 8-10* is/are rejected.

7)☒ Claim(s) *2,3,5-7 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *031004 &031704*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Restriction/election

1. Applicant's election with traverse of Group I (claims 1-11) filed on June 21, 2005 has been acknowledged. The traversal is on the ground(s) that the search would allegedly not cause undue burden of search for Examiner and stated that the Office action fails to list any such "other and materially different products" in the process as claimed.

This is not found persuasive because of search has already established by the different classification of the inventions I and II drawn to a method of forming integrated circuit device and an apparatus of an integrated circuit device, which are completely distinct between a process and a process of the semiconductor device. Furthermore, a step of removing the thick layer of polysilicon in the array region is not required in the product .

The requirement is still deemed proper and is therefore made FINAL.

Claims 12-20 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to non-elected inventions, there being no allowable generic or linking claim.

Information Disclosure Statement

2. The office acknowledges receipt of the following items from the applicant:

Information Disclosure Statement (IDS) filed on March 10, 2004 and March 17, 2004.

Specification

3. The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

4. Claims 1 and 10 are objected to because of the following reasons:

In claim 1, line 5, replace a term "form" by – forming --, line 8, "remove" by – removing --, lines 9-10, "deposit" by – depositing --.

In claim 10, lines 9-12 "afterforming word lines and gate electrodes in the arry region and support region forming sidewall spacers on sidewalls thereof" is indefinite. Correction is required.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1 and 9 are rejected under 35 U.S.C. 102 (b) as being anticipated by Huang (U.S. Patent No. 6,074,908).

Regarding claim 1, Huang discloses a method of forming integrated circuit device including at least one semiconductor memory array region and logic circuits including a support region including the steps as follows:

form a thick deposit of polysilicon (16, Fig. 1) in both the array region (M, Fig. 1) where word lines are located and where the support region (L, Fig. 1) where the logic circuits are located;

then removing the thick layer of polysilicon (16, Fig. 1) only in the array region (M, Fig. 2) then depositing a thin layer of polysilicon (25, Fig. 3) in both the array region and the support region;

then depositing a metallic conductor (26, Fig. 3) coating including at least an elemental metal layer portion over the thin layer of polysilicon (25, Fig. 3);and

then forming word lines andgate electrodes in the array region and support region respectively. (Fig. 8).

Regarding claim 9, Huang discloses a capping silicon nitride layer (30, Fig. 3 and col. 5, lines 8-9) is formed over the metal layer before forming word lines and gate electrodes in the array region (M, Fig. 3) and support region (L, Fig. 3).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 4 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang in view of Tseng (U.S. Patent No. 5,843,821).

Huang discloses all the features of the claimed invention as discussed above, but does not disclose the thin layer of polysilicon comprises amorphous silicon, wherein a gate oxide layer is formed over the device after formation of the sacrificial polysilicon layer.

Tseng, however, discloses the thin layer of polysilicon comprises amorphous silicon, wherein a gate oxide layer (36A, Fig. 3) is formed over the device after formation of the sacrificial polysilicon layer (36, Fig. 2) [col. 5, lines 56].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to modify the above discussed teaching of Huang as taught by Tseng for a purpose of improving self-aligned node contact with smaller size.

7. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Huang in view of Applicant's Figs. 1-2.

Huang discloses all the features of the claimed invention as discussed above, but does not disclose forming the integrated circuit device on a semiconductor substrate with a polysilicon stud is in a trench in the semiconductor substrate under an electrically conductive word line with the stud being electrically insulated from the substrate by dielectric material on sidewalls of the trench and an Array Top Oxide (ATO) layer formed above the substrate aside from the polysilicon stud; and after forming word lines and gate electrodes in the array region and support region; and forming sidewall spacers on sidewalls thereof.

Applicant's Figs. 1-2, however, discloses forming the integrated circuit device on a semiconductor substrate with a polysilicon stud is in a trench in the semiconductor substrate under an electrically conductive word line with the stud being electrically insulated from the

substrate by dielectric material on sidewalls of the trench and an Array Top Oxide (ATO) layer formed above the substrate aside from the polysilicon stud; and after forming word lines and gate electrodes in the array region and support region; and forming sidewall spacers on sidewalls thereof.

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to modify the above discussed teaching of Huang as taught by Applicant's Prior Arts for a purpose of improving a process of forming integrated circuit device.

Allowable Subject Matter

8. The following is a statement of reason for the indication of allowable subject matter:

Claims 2-3, 5-7 and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claim.

None of the prior art made of record does not disclose the method begins with formation of a sacrificial polysilicon layer over the array region followed by formation of a gate oxide layer over the device, and performing the step of precleaning the device prior to the deposit of the thin layer of polysilicon as cited in claim 2 and the method begins with formation of a blanket sacrificial polysilicon layer over the array region followed by formation of a gate oxide layer over the device as cited in claim 5 and a step of precleaning is performed prior to of polysilicon the step of depositing the thin layer in both the array region and the support region as cited in claim 11.

Claims 3 and 7 are depend on claim 2 and claim 6 is depend on claim 5, then, they also would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claim.

Conclusion

9. Applicants are advised to cancel the non-elected claimsof Group II (claims 12-20) upon response to the nest Office action if the application is considered to be allowed.

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Bronner's 834 and Weis's 573 are cited interest.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuc T. Dang whose telephone number is (571) 272-1776. The examiner can normally be reached on 8:00 am-5:00 pm.

12. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on (571) 272-1787. The fax phone numbers for the organization where this application or proceeding is assigned are 571-273-8300 for regular communications and After Final communications.

13. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Phuc T. Dang PD

Primary Examiner

Art Unit 2818